IN THE CLAIMS

1. (Previously presented) A memory device for use with a memory controller, the memory device comprising:

a memory cell array adapted to store internal depth data of an object;

a compare circuit;

a line connecting the compare circuit to the memory cell array; and

a data modifying circuit distinct from the memory controller, the data modifying circuit including the compare circuit and being adapted to:

receive corresponding new external depth data of the object from the memory controller,

compare the new external depth data with the internal depth data, and

write the external depth data, via the connecting line, into the memory cell array over the internal depth data depending on the result of the comparison, and

output to the memory controller a status signal.

2. (Cancelled)

3. (Original) The memory device of claim 1, further comprising:

a first control pin for receiving a first control signal from the memory controller; and

a control circuit for transmitting the external depth data to the memory cell array thereby bypassing the data modifying circuit depending on a state of the first control signal.

4. (Cancelled)

5. (Currently amended) The memory device of claim 3 [[4]], wherein

the status signal is output through the first control pin.

6. (Previously presented) The memory device of claim 1, wherein the data modifying circuit includes

a register for storing the received new external depth data, wherein the compare circuit is adapted to compare the stored new external depth data with the internal depth data, and adapted to write the external depth data, via the connecting line, into the memory cell array depending on the result of the comparison.

7. (Original) The memory device of claim 6, wherein the compare circuit is further adapted to write the external depth data in the memory cell array if the external depth data is smaller than the internal depth data.

8. (Original) The memory device of claim 6, wherein the compare circuit is further adapted to output a status signal to the memory controller.

9. (Original) The memory device of claim 6, further comprising:

a second control pin for receiving a second control signal from the memory controller,

wherein the compare circuit compares the internal depth data with the stored external depth data in units of X bits when the second control signal is in a non-active state, and in units of NX bits when the second control signal is in an active state.

10. (Original) The memory device of claim 9, wherein

if the second control pin is in an inactive state, the compare circuit outputs to the memory controller:

a first status signal indicating that the lower X bits of the internal depth data have been modified, and

a second status signal indicating that the upper X bits of the internal depth data have been modified.

11. (Original) The memory device of claim 9, wherein

if the second control pin is in a non-active state, the compare circuit outputs to the memory controller a status signal indicating that NX bits of the internal depth data have been modified.

12. (Previously presented) A method of processing depth data of an object in a memory device controlled by a memory controller, the method comprising:

receiving external depth data of the object from the memory controller;

storing the received external depth data;

receiving a first control signal from the memory controller through a first control pin distinct from the memory controller;

determining a state of the first control signal;

if the state of the first control signal is determined to be inactive, writing the external depth data to a memory cell array within the memory device,

else if the state of the first control signal is determined to be active, receiving the stored external depth data and corresponding internal depth data stored in the memory cell array at a compare circuit that is distinct from the memory controller and connected via a line to the memory cell array comparing, the received data, writing from the compare circuit, via the connected line, the external depth data over the corresponding internal depth data into the memory cell array depending on the result of the comparison, and outputting to the memory controller a status signal indicating that the internal depth data has been modified;

receiving a second control signal from the memory controller through a second control pin distinct from the memory controller;

determining a state of the second control signal; and

if the state of the second control signal is determined to be inactive, comparing the internal depth data with the stored external depth data in units of X bits,

elseif the state of the second control signal is determined to be active, comparing the internal depth data with the stored external depth data in units of NX bits,

wherein comparing the internal depth data with the stored external depth data in units of NX bits further includes

outputting to the memory controller a status signal indicating that the NX bits of the internal depth data has been modified.

13. (Cancelled)

14. (Previously presented) The method of claim 12, wherein

writing the external depth data takes place if the comparison yields that the external depth data is smaller than the internal depth data.

15. (Previously presented) The method of claim 12, wherein

writing the external depth data takes place if the comparison yields that the external depth data is larger than the internal depth data.

16. (Cancelled)

17. (Previously presented) The method of claim 12, wherein comparing the internal depth data with the stored external depth data in units of X bits further includes

outputting to the memory controller a first status signal indicating that the lower X bits of the internal depth data have been modified, and

outputting to the memory controller a second status signal indicating that the upper X bits of the internal depth data have been modified.

18. (Original) The method of claim 17, wherein the first status signal is output through the first control pin, and the second status signal is output through the second control pin.

19. (Cancelled)

20. (Previously presented) The method of claim 12, wherein the status signal is output through one of the first and second control pins.

21-23 (Cancelled)

24. (Previously presented) The memory device of claim 1, further comprising a first control pin that directly connects the compare circuit to the memory controller.

25. (Previously presented) The memory device of claim 24, wherein the first control pin is adapted to receive a first control signal from the memory controller and to output a first status signal to the memory controller.

26. (Previously presented) The memory device of claim 25, further comprising a second control pin that directly connects the compare circuit to the memory controller.

27. (Previously presented) The memory device of claim 26, wherein the second control pin is adapted to receive a second control signal from the memory controller and to output a second status signal to the memory controller.